## 6.3 GHz Compact USB Real-Time Spectrum Analyzer

## **SAM-60 M3**

## **Product Brochure V1.0**

2023-10-18

- 9 kHz~6.3 GHz real-time spectrum analyzer
- Integrated 100 kHz-6.3 GHz analog signal generator (opt.)
- 100 MHz analysis bandwidth, 300 GHz/sec spectrum sweep speed, FPGA signal processing
- 1GHz phase noise: -114 dBc/Hz@10kHz
- Equipped with preamplifier, 1GHz DANL: -166.6 dBm/Hz
- Core module supported, weight 168g, size 142×54×16mm, power consumption 7-10W
- Highly compatible API interfaces and SAStudio4 GUI
- Compatible with ARM and x86 processors, Linux and Windows operating systems
- Operating temperatures range from -20 oC/-40 oC to 65 oC (option)
- Built-in OCXO (option), temperature drift≤0.15 ppm
- USB3.0/2.0 Type-C interface





Indicator test basis Hardwa	re Version: R5 API: 0.55.12	2 FPGA: 0.55.2	MCU: 0.55.9	SAS4: 1.55.57		
Frequency						
Frequency	0 kH-26 2 CH-					
Frequency Range	9 kHz~6.3 GHz					
Initial Frequency Accuracy	<1 ppm, supporting program manual correction					
Reference Clock	Internal or external, protection temperature drift<1 pp					
Spectrum Purity						
SSB Phase Noise		dBo	:/Hz			
Carrier Frequency	500 MHz	1 GHz	3 GHz	6 GHz		
1 kHz	-112.8	-107.5	-99.3	-93.1		
10 kHz	-120.6	-114.2	-103.6	-101.2		
100 kHz	-120.1	-112.5	-101.8	-99.3		
1 MHz	-134.1	-132.8	-127.7	-122.7		
Residual Response Spurious rejection on	Frequency Range	R.L.=0 dBm	R.L.=-20 dBm	R.L.=-50 dBm		
dBm, RBW =1 kHz, positive		-90	-104	-132		
peak detector	100MHz~6.3GHz	-90	-103	-111		
Residual Response Spurious rejection off	100kHz~100MHz	-79	-97	-120		
<u>, , , , , , , , , , , , , , , , , , , </u>	100MHz~6.3GHz	-90	-103	-111		
Image Frequency Suppression	>90 dBc (spurious rejecti	ion on, typical value), >35	dBc (spurious rejection	off, typical value)		
Local Oscillator Related Spurious	<-65 dBc (Offset Center F	Frequency +/- (N/M)*125	5MHz, N/M = 1,2,3,4,5)			
Signal Processing						
Analysis Bandwidth	Maximum 100 MHz, Dec	imate Factor:1				
IQ Data	125MSPS, Decimate fact	125MSPS, Decimate factor: 1,2,4,8,16,32,64128,256,512,1024,2048,4096 supported (FPGA)				
_	The built-in memory depth is 128 Mbytes					
	The built-in memory de	epth is 128 Mbytes		3upported (11 <b>3</b> 7.)		
Storage Depth	Supports continuous a	nd uninterrupted stora		eration rate is less t		
	Supports continuous a the bus bandwidth, and	nd uninterrupted stora d the storage depth is c		eration rate is less t		
External Trigger Response	Supports continuous a the bus bandwidth, and Maximum response freq	nd uninterrupted stora d the storage depth is c		eration rate is less t		
External Trigger Response Analog IF Output	Supports continuous a the bus bandwidth, and	nd uninterrupted stora d the storage depth is c		eration rate is less t		
External Trigger Response Analog IF Output	Supports continuous a the bus bandwidth, and Maximum response freq	nd uninterrupted stora d the storage depth is o uency 500 times/sec	only limited by the hard	eration rate is less t I disk capacity		
External Trigger Response  Analog IF Output  Amplitude  Maximum safe input power	Supports continuous a the bus bandwidth, and Maximum response freq	and uninterrupted stora d the storage depth is c uency 500 times/sec	only limited by the hard	eration rate is less t I disk capacity ≥ 0 dBm)		
External Trigger Response Analog IF Output Amplitude Maximum safe input power	Supports continuous a the bus bandwidth, and Maximum response freq	and uninterrupted stora d the storage depth is c uency 500 times/sec	only limited by the hard	eration rate is less t I disk capacity ≥ 0 dBm)		
External Trigger Response Analog IF Output Amplitude  Maximum safe input power (CW)	Supports continuous a the bus bandwidth, and Maximum response freq Not available  26 dBm	and uninterrupted stora d the storage depth is c uency 500 times/sec	only limited by the hard	eration rate is less t I disk capacity ≥ 0 dBm)		
External Trigger Response Analog IF Output Amplitude  Maximum safe input power (CW)  Maximum DC Voltage	Supports continuous a the bus bandwidth, and Maximum response freq Not available  26 dBm  10 dBm	and uninterrupted stora d the storage depth is c uency 500 times/sec	only limited by the hard	eration rate is less t I disk capacity ≥ 0 dBm)		
External Trigger Response Analog IF Output Amplitude  Maximum safe input power (CW)  Maximum DC Voltage  Display Range	Supports continuous a the bus bandwidth, and Maximum response frequency Not available  26 dBm  10 dBm  ±15 VDC	and uninterrupted stora d the storage depth is c uency 500 times/sec	only limited by the hard	eration rate is less t I disk capacity ≥ 0 dBm)		
External Trigger Response Analog IF Output Amplitude  Maximum safe input power (CW)  Maximum DC Voltage  Display Range  Amplitude Accuracy	Supports continuous a the bus bandwidth, and Maximum response freq Not available  26 dBm  10 dBm  ±15 VDC  DANL~26 dBm	and uninterrupted stora d the storage depth is cuency 500 times/sec  30 MHz~6.3 GHz and 100 kHz~30 MHz or process.	only limited by the hard	eration rate is less t I disk capacity ≥ 0 dBm)		
External Trigger Response Analog IF Output Amplitude  Maximum safe input power (CW)  Maximum DC Voltage  Display Range  Amplitude Accuracy  IF in-band spectrum ripple	Supports continuous a the bus bandwidth, and Maximum response freq Not available  26 dBm  10 dBm  ±15 VDC  DANL~26 dBm  ±1.5 dB	and uninterrupted stora d the storage depth is cuency 500 times/sec  30 MHz~6.3 GHz and 100 kHz~30 MHz or process.	only limited by the hard	eration rate is less t I disk capacity ≥ 0 dBm)		
External Trigger Response Analog IF Output Amplitude  Maximum safe input power (CW)  Maximum DC Voltage  Display Range  Amplitude Accuracy  IF in-band spectrum ripple  Reference level (R.L.)	Supports continuous a the bus bandwidth, and Maximum response frequency Not available  26 dBm  10 dBm  ±15 VDC  DANL~26 dBm  ±1.5 dB  ±1.75 dB (100 MHz analogous)	and uninterrupted storal the storage depth is converged to the storage de	the preamplifier off (R.L. reamplifier on (R.L. <0 dB	eration rate is less to disk capacity  ≥ 0 dBm)  sm)		
External Trigger Response Analog IF Output Amplitude  Maximum safe input power (CW)  Maximum DC Voltage Display Range Amplitude Accuracy IF in-band spectrum ripple Reference level (R.L.)  RF Preamplifiers	Supports continuous a the bus bandwidth, and Maximum response freq Not available  26 dBm  10 dBm  ±15 VDC  DANL~26 dBm  ±1.5 dB  ±1.75 dB (100 MHz analogue)  -50 dBm~23 dBm  Converting bands (free	and uninterrupted storal the storage depth is converged to the storage de	the preamplifier off (R.L. reamplifier on (R.L. <0 dB	eration rate is less to disk capacity  ≥ 0 dBm)  sm)		
External Trigger Response Analog IF Output Amplitude  Maximum safe input power (CW)  Maximum DC Voltage  Display Range  Amplitude Accuracy  IF in-band spectrum ripple  Reference level (R.L.)	Supports continuous a the bus bandwidth, and Maximum response freq Not available  26 dBm  10 dBm  ±15 VDC  DANL~26 dBm  ±1.5 dB  ±1.75 dB (100 MHz analogous) -50 dBm~23 dBm  Converting bands (free automatically turn on continuous)	and uninterrupted storal the storage depth is converged to the storage de	the preamplifier off (R.L. reamplifier on (R.L. <0 dB equipped with preamplifier on (B.L. $\geq$ 10 dBm)	eration rate is less to disk capacity  ≥ 0 dBm)  sm)		

	T	-					
	Frequency Range		R.L.= 0 dBm (IFGainGrade = 3)			20 dBm Grade = 3)	R.L.=-50 dBm (IFGainGrade = 3)
Display Average Noise Level (DANL)	9 kHz		-122		-1	134	-149
dBm/Hz	100kHz		-132		-:	140	-152
RBW=10kHz RMS detector	100 MHz~3.0	GHz	-129		-:	145	-161
	3.0 GHz~6.3 GHz		-129			141	-158
Standard Spectrum Analysis	3.0 0112 0.3	123		•	- 1 -	130	
Detector	Positive peak, Negative peak, Sampling, Average, RMS, Max Power						
RBW	0.1 Hz~10 MHz						
VBW	0.1 Hz~10 MHz						
Trace Function	Sample, Positive Peak, Negative Peak, Local average, Maximum hold, Minimum hold, Average						
Data Chart	SAStudio4 software provides regular spectrum, waterfall chart, and historical trace						
	310.3 GHz/s FPGA RBW≥250 kHz, B-Nuttal window, spurious rejection: Standard						
Sweep speed - Standard	150.2 GHz/s	FPGA	RBW=25	50 kHz, B	-Nuttal win	dow, spurious re	ejection: Enhanced
Spectrum Analysis	38.7 GHz/s	FPGA	FPGA RBW=30 kHz, B-Nuttal window, spurious rejection: Enha			ection: Enhanced	
	1.8 GHz/s	CPU	RBW=1	kHz, B-N	uttal windo	w, spurious reje	ction: Enhanced
Detection Analysis/Zero Span							
Highest Time Resolution	8 ns						
Maximum Analysis Bandwidth	100 MHz						
Detector	Positive peak, Negative peak, Sampling, Average, RMS, Max Power						
Real Time Spectrum Analysis							
FFT Analysis	Variable point FFT engine implemented by FPGA. frame rate compression and trace detection are supported. There is strictly no gap and overlap between FFT frames  FFT refresh rate=10 ^ 9 ns/(N * D * 8 ns); POI = 2*N*D*8ns N is the number of FFT points (2048, 1024,512,256,128,64,32), and D is the decimate factor (1, 2, 4, 8,)						
	Typical Settings		F	FFT Refresh Rate			POI
	N = 2048, D = 1		61,0	61,035 times /second		32.768 us	
	N = 32, D = 1		3,906	3,906,250 times /second		0.512 us	
Real-time Analysis Bandwidth	100 MHz						
Window Function	B-Nuttall, FlatTop						
RBW	14.73 MHz-3.59 kHz (Flattop window); 7.81 MHz~1.90 kHz (B-Nuttall); 13 grades for each window type						
Amplitude Resolution	0.75 dB						
Signal generator (option)							
Frequency range	100 kHz~6.3 GH	z, 10 Hz for	each step	)			
Power range	-50 dBm~0 dBm, 0.25 dB for each step						
VSWR	<2.0:1			30 MHz	~6.3 GHz		
Non-harmonic spurs	<-50 dBc						
Harmonic wave	100 kHz~30 MHz	0 MHz 30 MHz~1.6 GHz		1.6 GH	z~3 GHz	3 GHz~3.2 GH	z 3 GHz~6.3 GHz
Second harmonic	<-10 dBc	<-10			O dBc	<-20 dBc	<-20 dBc
Third harmonic and above	<-10 dBc	<-10			O dBc	<-20 dBc	<-20 dBc
2	100 kHz~30 MHz	Į.		>90 dBc			
Signal leakage to receiver	30 MHz~3 GHz			>80 dBc			
	3 GHz~6.3 GHz			>70 dBc			
	7/0 ubc						

General					
Input and Output	Power Supply	Type-C (1), dedicated power supply port, please provide 5V 2A p power supply capacity Allowable voltage range: 4.75~5.25 V, ripple less than 200 mVpp			
	Data	Type-C (2), USB3.0 (USB2.0 Available but bandwidth limited)			
	RF input	SMA (F), Input impedance 50 $\Omega$			
	External reference clock input	MCX (F) (1), amplitude $\geq$ 1.5 Vpp, input impedance 330 $\Omega$			
	External reference clock output	Not supported			
	External trigger input	Integrated in MUXIO, 3.3 V CMOS, input: high impedance			
	External trigger output	Integrated in MUXIO (type C), 3.3 V CMOS			
	Analog IF output	Not supported			
Power Consumption	Peak: 10 W, typical: 7 W~10 W, Power port (5V 2A Max), Data port (5V 1A Max)				
Operating Temperature	0~50 °C/0~70 °C (Standard temperature class)				
(ambient temperature	-20~65 °C/-20~85 °C (Extended Temperature Class Option) (plastic enclosure and fan not included)				
/device core temperature)	-40~65 °C/-40~85 °C (Wide Temperature Class Option) (plastic enclosure and fan not included)				
C	-20~70 °C (Standard temperature class)				
Storage Temperature (ambient temperature)	-40~85 °C (Extended temperature class and wide temperature options) (plastic enclosure and fan not included)				
Size and Weight	142x54x16mm, 168 g (Excluding protective case and structural fittings, including connector length) 156x62x22mm, 296 g (Including protective case and structural fittings, including connector length)				
Packaging and Accessories	Flash drive * 1, USB 3.0 cable * 2, Power adapter * 1				

<sup>\*</sup>The typical values of the indicators are applicable for the following conditions: (1) Start up and warm up for 20 minutes; (2) Ambient temperature 25 °C (core temperature 50 °C); (3) SWP-Spurious rejection on; (4) 100MHz analysis bandwidth and IFGainGrade=3; (5) The user shall provide the necessary heat dissipation conditions to ensure that the ambient temperature and the core temperature of the equipment are within the rated range at the same time.

Code	Option	Explanation
01	Built-in OCXO reference clock (hardware opt.)	Providing a reference clock with better stability than the standard configuration, with a temperature drift of<0.15 ppm, increasing the overall power consumption by 0.8 W.
02	Built-in analog signal generator	100 kHz-6.3 GHz signal generator
10	IO extension board (accessory)	Converting the MUXIO interface into multiple MMCX and board to wire connector to facilitate the connection of trigger input, output, and other signals.
11	External GNSS (accessory)	Standard GNSS module connected to MUXIO.
12	External high precision GNSS (accessory)	High precision GNSS module connected to MUXIO.
13	External GNSS disciplined OCXO reference clock (accessory)	Providing GNSS disciplined reference clock and 1PPS, increasing the overall power consumption by 1.1W.
20	Extended temperature class (hardware opt.)	- 20~65 °C/- 20~85 °C(Extended temperature class opt.)
21	Wide temperature class (hardware opt.)	- 40~65 °C/- 40~85 °C(Wide temperature class opt.)

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