Synthesized Clock Generator

CG635 — DC to 2.05 GHz low-jitter clock generator

CG635 Synthesized Clock Generator

- **Clocks from DC to 2.05 GHz**
- **Random jitter <1 ps rms**
- **16 digits of frequency resolution**
- **80 ps rise and fall times**
- **CMOS, PECL, ECL, LVDS, RS-485 outputs**
- **Phase control and time modulation**
- **PRBS for eye-pattern testing (opt.)**
- **OCXO and rubidium timebase (opt.)**

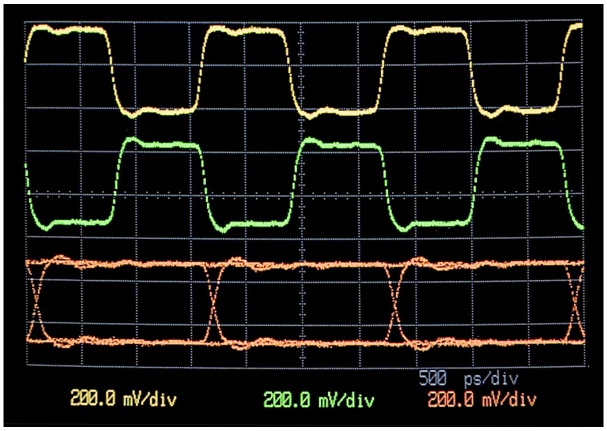
The CG635 generates extremely stable square wave clocks between 1 µHz and 2.05 GHz. The instrument's high frequency resolution, low jitter, fast transition times, and flexible output levels make it ideal for use in the development and testing of virtually any digital component, system or network.

Clean clocks are critical in systems that use high-speed ADCs or DACs. Spurious clock modulation and jitter create artifacts and noise in acquired signals and in reconstructed waveforms. Clean clocks are also important in communications systems and networks. Jitter, wander, or frequency offsets can lead to high bit error rates, or to a total loss of synchronization. The CG635 can provide the clean, stable clocks required for the most critical applications.

Output Drivers

The CG635 has several clock outputs. The front-panel Q and $\overline{Q}$ outputs provide complementary square waves at standard logic levels (ECL, PECL, LVDS or +7 dBm). The square wave amplitude may also be set from 0.2 V to 1.0 V, with an offset between −2 V and +5 V. These outputs operate from DC to 2.05 GHz, have transition times of 80 ps, a source impedance of 50 Ω, and are intended to drive 50 Ω loads. Output levels double when these outputs are unterminated.

The front-panel CMOS output provides square waves at standard logic levels. The output may also be set to any



Clock and PRBS signals at 622.08 MHz

The scope traces show complementary clock and PRBS outputs at 622.08 Mb/s with LVDS levels. The clock and PRBS outputs have transition times of 80 ps and jitter less than 1 ps (rms). The optional PRBS generator provides random data up to 1.55 Gb/s for eye-pattern testing of high-speed data channels.

amplitude from 0.5 V to 6.0 V. The CMOS output has transition times of less than 1 ns and operates up to 250 MHz. It has a 50 Ω source impedance and is intended to drive high impedance loads at the end of any length of 50 Ω coax cable.

A rear-panel RJ-45 connector provides differential square wave clocks on twisted pairs at RS-485 levels (up to 105 MHz) and LVDS levels (up to 2.05 GHz). This output also provides ±5 VDC power for optional line receivers (CG640 to CG649). The clock outputs have 100 Ω source impedances and are intended to drive shielded CAT-6 cable with 100 Ω terminations. The differential clocks may be used directly by the target system, or with optional line receivers that provide complementary logic outputs on SMA connectors.

Choice of Timebases

The standard crystal timebase has a stability of better than 5 ppm. The CG635's 10 MHz timebase input allows the instrument to be phase-locked to an external 10 MHz reference. The 10 MHz output may be used to lock two CG635s together.

There are two optional timebases. An oven-controlled crystal oscillator (OCXO) provides about 100 times better frequency stability than the standard crystal oscillator. A rubidium frequency source provides about 10,000 times better stability. Either optional timebase will substantially reduce the low-frequency phase noise of the synthesized output.

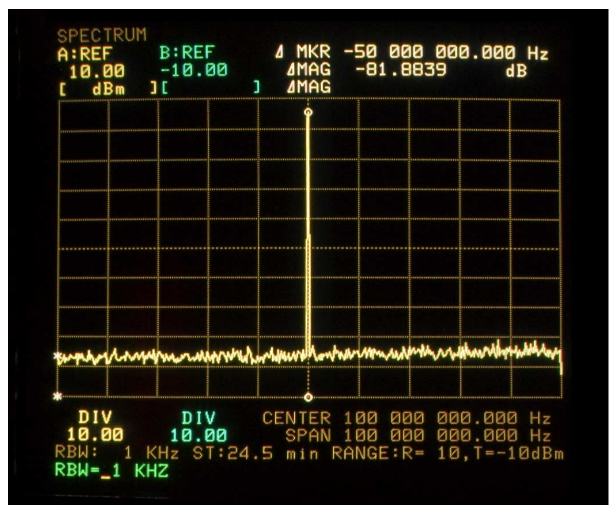
Phase and Time Modulation

The clock phase can be adjusted with high precision. The phase resolution is one degree for frequencies above 200 MHz, and increases by a factor of ten for each decade below 200 MHz, with a maximum resolution of one nano-degree. This allows clock edges to be positioned with a resolution of better than 14 ps at any frequency between 0.2 Hz and 2.05 GHz.

The timing of clock edges can be modulated over ±5 ns via a rear-panel time-modulation input. The input has a sensitivity of 1 ns/V and a bandwidth from DC to over 10 kHz, allowing an analog signal to control the phase of the clock output. This feature is very useful for characterizing a system's susceptibility to clock modulation and jitter.

For Every Application

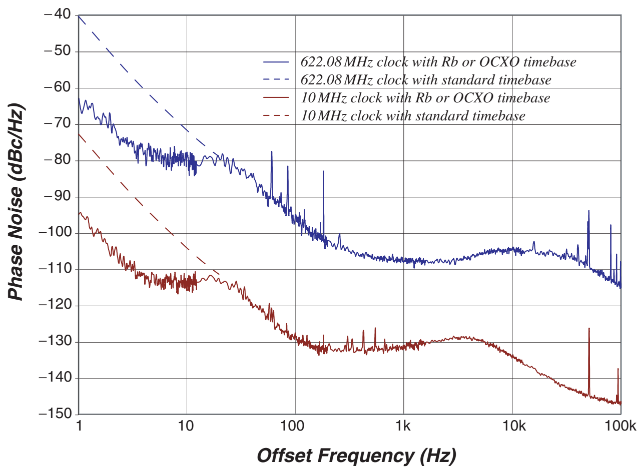
With its exceptionally low phase noise and high frequency resolution, the CG635 replaces RF signal generators in many applications. Front-panel outputs provide square waves up to +7 dBm — ideal for driving RF mixers. Should your application require sine waves, in-line low-pass filters are commercially available to convert the CG635's square wave outputs to low distortion sine wave outputs.



RF Spectrum of a 100 MHz clock

This high resolution scan shows a 100 MHz span around a 100 MHz clock. Only two features are present: the clock at 100 MHz, and the spectrum analyzer's noise floor (around –82 dBc) everywhere else. The CG635's spur-free clock allows acquisition and reconstruction of waveforms with a high SFDR.

The CG635 can provide a wide range of clean, precise clocks for the most critical timing requirements. The instrument is an essential tool for demonstrating a system's performance with a nearly ideal clock, and for understanding a system's susceptibility to a compromised clock. The CG635 has the frequency range, precision, stability, and jitter-free performance needed to fulfill all your clock requirements.



Phase noise for 622.08 MHz and 10 MHz outputs

These graphs may be scaled by 20 dB/decade to estimate the phase noise at other frequencies. The CG635's low phase noise allows acquisition and reconstruction of waveforms with a low noise floor.

Ordering Information

CG635	Synthesized clock generator
Option 01	PRBS w/ complementary LVDS outputs on SMA
Option 02	OCXO timebase
Option 03	Rubidium timebase
CG640	CMOS (+5 Vcc) to 100 MHz
CG641	CMOS (+3.3 Vcc) to 500 MHz
CG642	CMOS (+2.5 Vcc) to 500 MHz
CG643	PECL (+5 Vcc) to 2050 MHz
CG644	PECL (+3.3 Vcc) to 2050 MHz
CG645	PECL (+2.5 Vcc) to 2050 MHz
CG646	RF (+7 dBm) to 2050 MHz
CG647	CML/NIM to 2050 MHz
CG648	ECL to 2050 MHz
CG649	LVDS to 2050 MHz
O635RMD	Double rack mount kit
O635RMS	Single rack mount kit

Rear-Panel Features

- *LVDS and RS-485 outputs (RJ-45)*
- *10 MHz reference input and output*
- *Universal input power supply*
- *GPIB and RS-232 interfaces*
- *Analog time modulation input*
- *PRBS generator with clock outputs (opt. 01)*
- *Optional line receivers with SMA outputs*

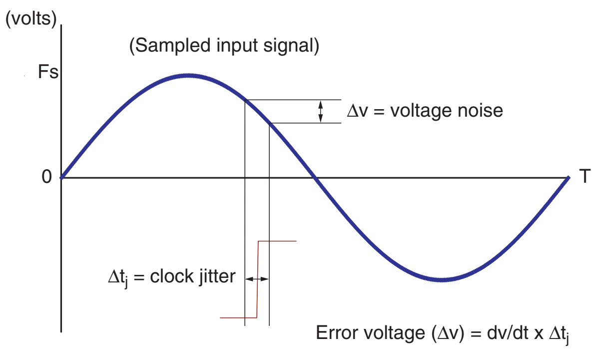
SRS Tech Note

Clock Jitter Matters

Square wave clocks are used in virtually every digital system. Two examples of applications that benefit from very stable clocks are discussed below.

Fast ADCs and DACs

When analog signals are digitized by ADCs or reconstructed by DACs, their finite resolution creates a quantization noise of about ½ LSB. Timing jitter also creates noise, which adds to the quantization noise. The figure below shows that a clock



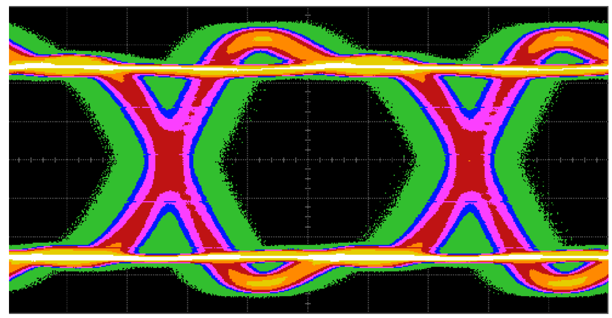
Sampling noise due to clock jitter

jitter of Δt_j causes a sampling noise of Δv, which is the product of the signal slope and the clock jitter. This noise increases linearly with signal magnitude, signal frequency, and clock jitter.

To prevent clock jitter from degrading the overall noise, Δv should be smaller than the quantization noise. This can place severe requirements on the system clock. For example, to assure that $\Delta v <$ ½ LSB while digitizing a full-scale 10 MHz signal with a 14-bit ADC, a clock jitter of less than 1 ps is required.

High-Speed Data Transmission

Many systems transfer data at high rates over serial interfaces. Gigabit data rates, once limited to the domain of fiber optics and high-speed backplanes, are now commonplace in consumer applications. The figure below shows the eye-pattern of a high-speed digital data stream. Various noise sources can cause jitter, which narrows the interval (the "eye") during which the data is reliably a "1" or a "0".



Eye-pattern of 100k bits of a serial data stream

Looking at the eye-pattern, it may seem unlikely that a logic transition could be delayed by as much as half a unit interval (UI), and cause an error. However, for random jitter with an rms value of σ, the probability that the clock edge is more than 7.5σ from its mean position is about 6.5×10^{-14}, which is a typical bit-error-rate for a data transmission system. Hence, for reliable data transmission at 2 Gb/s, the jitter should be less than one fifteenth a UI, or about 33 ps.

Frequency

Range	DC, 1 µHz to 2.05 GHz
Resolution	16 digits ($f \geq 10$ kHz), 1 pHz ($f < 10$ kHz)
Accuracy	$\Delta f < \pm(2 \times 10^{-19} + \text{timebase error}) \times f$
Settling time	<30 ms

Timebase *(+20 °C to +30 °C ambient)*

Stability	<5 ppm (std. timebase)
	<0.01 ppm (Opt. 02 OCXO)
	<0.0001 ppm (Opt. 03 Rb timebase)
Aging	<5 ppm/yr. (std. timebase)
	<0.2 ppm/yr. (Opt. 02 OCXO)
	<0.0005 ppm/yr. (Opt. 03 Rb timebase)
External input	10 MHz ± 10 ppm, sine >0.5 Vpp, 1 kΩ
Output	10 MHz, 1.41 Vpp sine into 50 Ω

Phase Noise *(at 622.08 MHz)*

100 Hz offset	<–90 dBc/Hz
1 kHz offset	<–100 dBc/Hz
10 kHz offset	<–100 dBc/Hz
100 kHz offset	<–110 dBc/Hz

Jitter and Wander

Jitter (rms)	<1 ps (1 kHz to 5 MHz bandwidth)
Wander (p-p)	<20 ps (10 s persistence)

Time Modulation *(rear-panel input, 1 kΩ)*

Sensitivity	1 ns/V, ±5 %
Range	±5 ns
Bandwidth	DC to greater than 10 kHz

Phase Setting

Range	±720° (max. step size ±360°)
Resolution	<14 ps
Slew time	<300 ms

Q and $\overline{Q}$ Outputs

Outputs	Front-panel BNC connectors
Frequency range	DC to 2.05 GHz
High level	$-2.00\,V \leq V_{HIGH} \leq +5.00\,V$
Amplitude	$200\,mV \leq V_{AMPL} \leq 1.00\,V$
	$(V_{AMPL} \equiv V_{HIGH} - V_{LOW})$
Level resolution	10 mV
Level error	<1 % + 10 mV
Transition time	<100 ps (20 % to 80 %)
Symmetry	<100 ps departure from nominal 50 %
Source impedance	50 Ω (±1 %)
Load impedance	50 Ω to ground on both outputs
Pre-programmed levels	PECL, LVDS, +7 dBm, ECL

CMOS Output

Output	Front-panel BNC
Frequency range	DC to 250 MHz
Low level	$-1.00\,V \leq V_{LOW} \leq +1.00\,V$
Amplitude	$500\,mV \leq V_{AMPL} \leq 6.00\,V$
	$(V_{AMPL} \equiv V_{HIGH} - V_{LOW})$
Level resolution	10 mV
Level error	<2 % + 20 mV
Transition time	<1 ns (20 % to 80 %)
Symmetry	<500 ps departure from nominal 50 %
Source impedance	50 Ω (reverse terminates cable reflection)
Load impedance	Unterminated 50 Ω cable of any length
Attenuation (50 Ω load)	Output levels are divided by 2
Pre-programmed levels	1.2, 1.8, 2.5, 3.3 or 5.0 V

RS-485 Output

Output	Rear-panel RJ-45
Frequency range	DC to 105 MHz
Transition time	<800 ps (20 % to 80 %)
Clock output	Pin 7 and pin 8 drive twisted pair
Source impedance	100 Ω between pin 7 and pin 8
Load impedance	100 Ω between pin 7 and pin 8
Logic levels	$V_{LOW} = +0.8\,V$, $V_{HIGH} = +2.5\,V$
Recommended cable	Straight-through Category-6

LVDS Output *(EIA/TIA-644)*

Output	Rear-panel RJ-45
Frequency range	DC to 2.05 GHz
Transition time	<100 ps (20 % to 80 %)
Clock output	Pin 1 and pin 2 to drive twisted pair
Source impedance	100 Ω between pin 1 and pin 2
Load impedance	100 Ω between pin 1 and pin 2
Logic levels	$V_{LOW} = +0.96\,V$, $V_{HIGH} = +1.34\,V$
Recommended cable	Straight-through Category-6

PRBS (Opt. 01) *(EIA/TIA-644)*

Outputs	PRBS, –PRBS, CLK and –CLK
Frequency range	DC to 1.55 GHz
Level	LVDS on rear-panel SMA jacks
PRBS generator	$x^7 + x^6 + 1$ for a length of $2^7 - 1$ bits
Transition time	<100 ps (20 % to 80 %)
Load impedance	50 Ω to ground on all outputs

General

Computer interfaces	GPIB and RS-232 std. All functions can be controlled through either interface.
Non-volatile memory	Ten sets of instrument configurations can be stored and recalled.
Power	90 to 264 VAC, 47 to 63 Hz, 50 W
Dimensions, weight	8.5" × 3.5" × 13" (WHD), 9 lbs.
Warranty	One year parts and labor